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## Search History

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L8: Entry 10 of 158 File: USPT Jun 4, 2002

DOCUMENT-IDENTIFIER: US 6400605 B1
TITLE: Method and system for pulse shaping in test and program modes

Detailed Description Text (3):
During a normal-mode operation, the input voltage 11 fluctuates between 0 to 5 volts, representing the nominal Vcc operating range. At that voltage range, the input voltage 11 is not at a sufficient high voltage level for the detection by either first voltage level detector 14 or second voltage level detector 15. Consequently, the high-level switch 12 is in an OFF state. To enter a test mode of integrated circuit 10, the test input voltage 11 is increased to a high-level voltage, e.g. 10 volts. The 10 volt in this instance represents a voltage level in which the first voltage level detector 14 detects test input voltage 11.

Detailed Description Text (13):
FIG. 3 is a flow diagram illustrating a dual level voltage sense method 50. Integrated circuit 10 receives 51 input voltage 11 for feeding to first voltage level detector 14, second voltage level detector 15, and high-voltage switch 12. First voltage level detector 14 detects 52 if input voltage 11 is sufficiently high to reach a first predetermined high voltage level, e.g. 10 volts. If input voltage 11 has reached a sufficient voltage level as set forth by the first predetermined high-level voltage, integrated circuit 10 enters 54 into a test mode. Data and addressing information are received 55 via interface control circuit 16. Integrated circuit 10 undergoes 56 testing or verification process for a period of time. However, if input voltage has not risen sufficiently to near or at first predetermined high voltage, integrated circuit 10 remains 53 in normal mode.

CLAIMS:

1. An integrated circuit, comprising:

an input pin for receiving a predetermined high-voltage program level during a program mode;

a first voltage-level detector for detecting a predetermined high-voltage test level, the integrated circuit entering into a test mode when an incoming voltage signal at the input pin rises to the predetermined high-voltage test level;

a second voltage level detector, coupled to the first voltage-level detector, for detecting the predetermined high-voltage program level, the integrated circuit entering the program mode when an incoming voltage at the input pin rises to the predetermined high-voltage program level; and

a high impedance circuit for gradually ramping up the predetermined high-voltage program level preventing damage caused to electrical erasable cells in the integrated circuit.

11. A method for programming an integrated circuit, comprising the steps of:

detecting a predetermined high-voltage test level from an input signal to place the integrated circuit in test mode;

detecting a predetermined high-voltage program level from the input signal to place the integrated circuit in program mode; and

ramping up gradually of the predetermined high-voltage program level preventing causing damage to electrical erasable cells in the integrated circuit.

test mode circuit.

Detailed Description Text (5):
Referring now to the detailed schematic of FIG. 3, test mode circuit 44 includes a high voltage detector 60 having an input for receiving the OEBPAD signal on node 22 and an output designated NODE2. The input to the high voltage detector 60 is an integrated circuit pin coupled to both the test mode circuit 44 and to other circuitry not forming part of the test mode circuit. A modified Schmitt trigger 62 has an input coupled to the output of the high voltage detector 60 at NODE2 and an output designated NODE3. A latch 68, 70 has an input stage 68 and a latch stage 70. The input stage 68 is used to prevent a reset condition in latch stage 70 during the test mode until a power-down condition occurs. An input of the input stage 68 is designated SCHMON, which is also coupled to an input of the modified Schmitt trigger 62. The output of input stage 68 is coupled to the input of the latch stage 70. The output of latch stage 70 is coupled through inverters m33 and m34 for providing the BURNIN test mode signal in a test operational mode at node 34. An inverter m21 generates the SCHMON signal, which is used to disable the high voltage detector 60 and Schmitt trigger 62 such that substantially all of the active current flow in those circuit blocks is eliminated in a normal operational mode. Inverter m21 receives the POR control signal on node 32 from power detect circuit 48. In FIG. 3, a glitch filter consisting of inverter string 64, logic gate m15, and inverter m16 is interposed between the output of the modified Schmitt trigger 62 and the input to input stage 68, which is used filter extraneous pulses and glitches in order to prevent a false entry into the test mode.

Detailed Description Text (17):
Test mode circuits 44 and 46, therefore, are used to detect an extra-high voltage level on a particular input pin of an integrated circuit. An extra-high level is defined to be a voltage significantly higher than the operating VDD voltage, for example three volts higher. High voltage detector 60 detects the extra-high level by employing two diodes in series which feed a modified Schmitt trigger inverter circuit 62. Once the input pin 22 or 26 rises about two diode drop voltages above VDD, the Schmitt trigger circuit 62 switches, causing the EH signal to go high. The EH signal feeds a latch 68, 70, which is power-gated with the POR control signal via inverter m21. As long as the integrated circuit has not been accessed POR will remain low and the state of the EXTRAHIGH signal will determine the logic state of the latch 68, 70. When the EH signal goes high, it will set latch 68, 70 and cause either the BURNIN signal (test mode circuit 44) or the PDDISABLE signal (test mode circuit 46) to go high. These signals are the ones that control the particular corresponding circuit block in the rest of the integrated circuit during the special test mode.

Detailed Description Text (19):
Once POR goes high for the first access, the Schmitt trigger circuit 62 is disabled from reacting to any more inputs. This is achieved by turning off device m10, which cuts off the ground path for the modified Schmitt trigger circuit 62. To prevent any floating nodes from occurring, device m12 is turned on, causing NODE3 to be pulled up to the VDD voltage level for the duration of the power-up condition. Also note that device m5 is turned off at this point to decrease the current being drawn through the series devices m2, m3, and m4 in high voltage detector 60. By turning off the Schmitt trigger circuit 62 and the high voltage detector 60, all active current is eliminated in the entire test mode circuits 44 and 46; only leakage current will continue to flow. The POR signal is designed so that it will not activate during normal operation until VDD is detected to be very low. Devices m17, m18, m19, and m20 are used to filter out any short glitches that might possibly occur on the EH signal. Devices m6 and m13 at the input and output of the Schmitt trigger circuit 62 are used to help keep NODE2 at ground and NODE3 coupled to VDD during power up, which helps to keep the EH signal at ground. Finally, device m1, located at the input of high voltage detector 60, is used solely for the purpose of ESD input protection. The operation of test mode circuits is further described

below with reference to the timing diagrams of FIGS. 5-8 and FIGS. 10-11.

Detailed Description Text (38):
In sum, an operating method for a test circuit has been described that includes the steps of detecting a high voltage input using a high voltage detector circuit, providing a test mode signal in a test operational mode, and disabling the high voltage detector circuit such that substantially all of the active current flow is eliminated in a normal operational mode. The test operational mode is prevented from reverting to the normal operational mode until a power-down condition occurs.

CLAIMS:

4. A test mode circuit as in claim 1 in which the input to the high voltage detector comprises an integrated circuit pin coupled to both the test mode circuit and to other circuitry not forming part of the test mode circuit.

6. A test mode circuit as in claim 5 in which the high voltage detector comprises:

a first diode having an anode forming the input and a cathode;

a second diode having an anode coupled to the cathode of the first diode and an anode forming the output;

a first transistor having a drain coupled to the output, a gate coupled to a source of power supply voltage, and a source; and

a second transistor having a drain coupled to the source of the first transistor, a gate forming the control node, and a source coupled to ground.

8. A test mode circuit as in claim 5 further comprising a diode having a cathode coupled to the input of the high voltage detector and an anode coupled to ground.

10. A test mode circuit as in claim 5 further comprising a capacitor coupled between the output of the high voltage detector and ground.

L8: Entry 13 of 158 File: USPT Feb 12, 2002

DOCUMENT-IDENTIFIER: US 6347381 B1
TITLE: Test mode circuitry for electronic storage devices and the like

Brief Summary Text (6):
The test circuitry typically contains a high voltage detection circuit for detecting the supervoltage on the input pin. For example, referring to FIG. 1, there is shown a prior art high voltage detection circuit 10 for detecting a supervoltage on an input pin 12. The high voltage detection circuit 10 includes a diode stack 14, a weak load transistor (i.e., a transistor that is biased and/or dimensioned so as to conduct only a relatively small amount of current) 16, and a series of inverters 18. If no supervoltage is applied to input pin 12, the diodes in the diode stack 14 typically cannot become forward biased and the weak load transistor 16 maintains node N1 in a low state. The signal at node N1 is then buffered through the series of inverters 18 so as to cause the output signal HVOUT to be in an inactive low state. However, if a supervoltage is applied to input pin 12, the diodes in the diode stack 14 can become forward biased and node N1 can be brought to a high state. The signal at node N1 is then buffered through the series of inverters 18 so as to cause the output signal HVOUT to be brought to an active high state. When the output signal HVOUT is active high, the rest of the test circuitry (not shown) places the electronic storage device into the test mode.

Brief Summary Text (7):
There are problems associated with the above-described high voltage detection circuit 10. For example, because input pin 12 is connected to a source/drain junction of the diode stack 14, pin leakage can become an issue and the source/drain junction can become forward biased. Also, the numerous diodes in the diode stack 14 are very process sensitive. Thus, accidental entry into or exit from the test mode is possible at some process corners. In fact, this is even likely since, as previously indicated, the electronic storage device is tested over a wide range of predetermined measurement conditions. Further, a current path can exist on some process/voltage corners for the supply voltage. That is, at high VCC (hot temperature) and a minimum transistor threshold corner, node N1 may not be at ground and the transistors in the first inverter in the series of inverters 18 may have some crowbar current. Additionally, the entire circuit is latch-up sensitive due to the range of voltages over which node N1 can reside.

Brief Summary Text (9):
In view of the foregoing, it would be desirable to provide test mode circuitry which overcomes the above-stated problems. More particularly, it would be desirable to provide test mode circuitry having a reliable high voltage detection circuit and/or a time-out feature disable circuit for allowing electronic storage, or other, devices to be tested in a more thorough and efficient manner.

Detailed Description Text (2):
Referring to FIG. 2A, there is shown a schematic diagram of a high voltage detection circuit 100 for detecting a supervoltage on an input pin 102 in accordance with the present invention. The high voltage detection circuit 100 includes a first inverter 104, a NOR gate 106, a first weak load N-channel transistor (i.e., a transistor that is biased and/or dimensioned so as to conduct only a relatively small amount of current) 108, a first P-channel transistor 110, a

second P-channel transistor 112, a second weak load N-channel transistor 114, a third P-channel transistor 116, a body tapped N-channel transistor 118, a schmitt trigger 120, and a series of inverters 122. For purposes of this detailed description, the high voltage detection circuit 100 is designed to be functional for a burn-in test mode.

Detailed Description Text (3):
During the burn-in test mode, a power down (PD) input signal is typically in an inactive low state and a stress (STRESS) input signal is typically in an inactive high state. The state of the PD input signal indicates the level of the supply voltage (VCC). That is, when the supply voltage is above a predetermined minimum operating voltage level (e.g., 4.5 volts), the PD input signal is in an inactive low state. The state of the STRESS input signal indicates whether or not a stress mode is active. That is, when the device which incorporates the high voltage detection circuit 100 is not in a stress mode (i.e., a programmable stress test mode), the STRESS input signal is in an inactive high state. As described in detail below, the body connection (BODY) to the body tapped N-channel transistor 118 is tied to either the source connection (SOURCE) to the body tapped N-channel transistor 118, or to VSS.

Detailed Description Text (6):
At this point it should be noted that when the PD input signal is in the active high state or the STRESS input signal is in the active low state, the logic of the first inverter 104 and the NOR gate 106 cause the first P-channel transistor 110 to be on, the first weak load N-channel transistor 108 to be off, and node N1 to be at VCC. Since the source connection (SOURCE) to the body tapped N-channel transistor 118 can never be above VCC, the third P-channel transistor 116 will be off and node N2 will be at VSS. In this state, the high voltage detection circuit 100 consumes no DC current and the test mode cannot be entered.

Detailed Description Text (9):
In view of the foregoing, it is apparent that the high voltage detection circuit 100 provides improved operation over process corners and operating corners (temperature and voltage). It also prevents pin leakage, accidental test mode entry, and reduced latch-up sensitivity.

Detailed Description Text (12):
The long cycle enable circuit 200 is operative to cause a long cycle (LC) output signal to be brought to an active low state whenever any of the input signals are active. In the context of the burn-in test mode, the LC output signal is brought to an active low state whenever the BURN-IN signal from the high voltage detection circuit 100 is in an active high state. That is, when the LCT input signal is in an inactive low state and the STRESS input signal is in an inactive high state, the LC output signal is in an active low state whenever the BURN-IN signal from the high voltage detection circuit 100 is in an active high state. Conversely, when the LCT input signal is in an inactive low state and the STRESS input signal is in an inactive high state, the LC output signal is in an inactive high state whenever the BURN-IN signal from the high voltage detection circuit 100 is in an inactive low state.

L8: Entry 3 of 158 File: USPT Jul 29, 2003

DOCUMENT-IDENTIFIER: US 6600685 B2
TITLE: Semiconductor memory device having test mode

Brief Summary Text (8):
To meet such a demand, a semiconductor memory device has recently been developed which is configured to automatically enter a test mode when a high voltage is applied to an input pin. The semiconductor memory device has a high-voltage detection circuit connected to its input pin to detect the application of a voltage higher than the normal operating voltage (Vcc). For example, with Vcc=3.3 V, a test is carried out when a voltage of not less than 6.5 V is applied to the input pin. With such a semiconductor memory device, packaged final products can be tested without using a special input pin. Accordingly, this kind of semiconductor memory device has come into widespread use.

Detailed Description Text (11):
Therefore, the excess addresses are used as address inputs for entering the test mode. Namely, an excess address or set of addresses is used as a particular signal. This allows tests to be performed as in normal memory operations even in packaged final products and without the need for a special input pin or high-voltage detection circuit.

Detailed Description Text (14):
As described above, the present embodiment allows packaged final products to be subjected to tests without the need for a special input pin or high-voltage detection circuit. That is, the test mode can be entered by externally applying excess addresses which are not used to access memory cells. In this way, the necessity for a special input pin and high-voltage detection circuit to enter the test mode is eliminated, allowing packaged final products to be tested with ease. In addition, not only can malfunction due to noise be prevented, but also the problem of reliability resulting from reducing the thickness of the gate insulating film can be eliminated.

L8: Entry 21 of 158 File: USPT Jun 5, 2001

DOCUMENT-IDENTIFIER: US 6243839 B1
TITLE: Non-volatile memory system including apparatus for testing memory elements by writing and verifying data patterns

Detailed Description Text (15):
The circuit of FIG. 3 is activated by application of a high voltage to two or more terminals 700 and 702 of the memory system from an external source. These terminals are non-dedicated terminals used during normal memory operations. Terminals 700 and 702 may include, for example, address terminal (pad) A10 and the write enable terminal WE. The magnitude of the high voltage applied to terminals 700 and 702 is chosen to be outside of the range of voltages which would typically be applied to those terminals during use of the terminals in normal (non-test mode) operation of the memory system. This is done to prevent an end user from unintentionally entering the test or special mode. The high voltage applied to terminals 700 and 702 is detected by detectors 706 and 708. A detector circuit suited for use in constructing detectors 706 and 708 is described in U.S. patent application Ser. No. 08/493,162, now U.S. Pat. No. 5,723,990 entitled, "Integrated Circuit Having High Voltage Detection Circuit", filed Jun. 21, 1995, the contents of which is hereby incorporated in full by reference.

CLAIMS:

10. A non-volatile flash memory device comprising:

an array of non-volatile memory cells;

a controller operable to perform an erase function on the non-volatile memory cells by executing a sequence of steps including a pre-program step of writing the non-volatile memory cells to a programmed state prior to executing an erase step;

a test mode detector circuit for detecting a high voltage applied to two external terminals and initiating a test mode operation;

flow control circuitry adapted to modify the sequence of steps of the controller during the test mode operation such that the erase step is not performed by the controller, and the pre-program step writes an externally provided test pattern to the non-volatile memory cells in place of the programmed state executed during the erase function; and

a bit register for storing data indicating if the externally provided test pattern is successfully programmed during the test mode.

15. A non-volatile flash memory device comprising:

an array of non-volatile memory cells;

a controller operable to perform an erase function on the non-volatile memory cells by executing a sequence of steps including a pre-program step of writing the non-volatile memory cells to a programmed state prior to executing an erase step;

a test mode detector circuit for detecting a high voltage applied to two external terminals and initiating a test mode operation;

flow control circuitry adapted to modify the sequence of steps of the controller during the test mode operation such that the erase step is not performed by the controller, and the pre-program step writes an externally provided test pattern to the non-volatile memory cells in place of the programmed state executed during the erase function;

a flow control register for storing data indicating a modified flow control operation for use by the flow control circuitry; and

an input data latch for storing the externally provided test pattern.

L8: Entry 6 of 158 File: USPT Mar 18, 2003

DOCUMENT-IDENTIFIER: US 6535447 B2
**** See image for Certificate of Correction ****
TITLE: Semiconductor memory device and voltage level control method thereof

Abstract Text (1):
The present invention discloses a semiconductor memory device and a voltage level control method thereof. The semiconductor memory device comprises multiple sub high voltage generators, multiple control circuits, a high voltage level detecting circuit, and a mode setting circuit. The multiple sub high voltage generators boost the high voltage level. The multiple control circuits control operations of each of the corresponding multiple sub high voltage generators responsive to each of corresponding high voltage detecting signals and to each of corresponding multiple control signals in the test mode. The high voltage level detecting circuit enabled by an active signal, detects the level drop of a high voltage and generates the high voltage detecting signal. The mode setting circuit sets the state of the multiple control signals responsive to the signals from the out side in the test mode. Performing the test by regulating the number of the multiple sub high voltage generators can prevent the semiconductor memory device from over kill. In addition, the test of the package state can be performed by enabling a few of the voltage generators than necessary for the full operation of the test mode.

CLAIMS:

1. A semiconductor memory device, comprising: a plurality of sub high voltage generators connected to receive a corresponding plurality of control signals, each sub high voltage generator for boosting a high voltage responsive to the corresponding control signal; a plurality of control circuits, each control circuit coupled to a corresponding sub high voltage generator for generating the corresponding control signal responsive to a high voltage detecting signal and a corresponding mode signals in a test mode; a high voltage level detect circuit for generating the high voltage detect signal responsive to detecting a high voltage level drop; and a mode setting circuit for generating a plurality of the corresponding mode signals responsive to external signals in the test mode.

L8: Entry 43 of 158 File: USPT Sep 8, 1998

DOCUMENT-IDENTIFIER: US 5804996 A
TITLE: Low-power non-resetable test mode circuit

Abstract Text (1):
A test mode circuit for an integrated circuit includes a high voltage detector having an input for receiving a high voltage signal, a Schmitt trigger having an input coupled to the output of the high voltage detector, a latch having an input coupled to the output of the Schmitt trigger and an output for providing a test mode signal in a test operational mode, and additional control circuitry for disabling the high voltage detector and Schmitt trigger so that substantially all of the active current flow in the high voltage detector and Schmitt trigger is eliminated in a normal operational mode. The test mode circuit further includes circuitry for preventing a reset condition in the latch during the test mode until a power-down condition occurs. A glitch filter is also included, which is interposed between the output of the Schmitt trigger and the input to the latch. An integrated circuit pin is coupled to both the test mode circuit and to other circuitry on the integrated circuit not forming part of the test mode circuit.

Brief Summary Text (3):
Referring now to FIG. 1, a prior art integrated circuit 10, such as a memory circuit, microprocessor, or the like, is shown having a main circuit 18 and a test mode circuit 16. The main circuit 18, for purposes of FIG. 1, is a circuit that includes the normal functional circuitry of integrated circuit 10. Main circuit 18 also includes external nodes or pins 14 not associated with the test mode circuit 16, which are inputs, outputs, or bi-directional pins. Typically, the test mode circuit 16 and main circuit 18 share a common external node 12. Node 12, under normal low voltage conditions, is typically an input or bi-directional pin for the main circuit 18. If a test mode is desired, a high voltage signal is applied to the test mode circuit 16 at node 12. The high voltage pulse is detected by test mode circuit 16, and a test mode signal is provided on node 20. Other techniques beyond the high voltage pulse are known for entering the test mode, such as placing a special code on node 12. The test mode signal changes the operation of main circuit 18 from a normal operating mode to a test mode. In the test mode, the characteristics of main circuit 18 or the input and output nodes 14 are changed as desired to affect the testing protocol.

Brief Summary Text (11):
According to the present invention a test mode circuit for an integrated circuit includes a high voltage detector having an input for receiving a high voltage signal, a Schmitt trigger having an input coupled to the output of the high voltage detector, a latch having an input coupled to the output of the Schmitt trigger and an output for providing a test mode signal in a test operational mode, and additional control circuitry for disabling the high voltage detector and Schmitt trigger so that substantially all of the active current flow in the high voltage detector and Schmitt trigger is eliminated in a normal operational mode. The test mode circuit further includes circuitry for preventing a reset condition in the latch during the test mode until a power-down condition occurs. A glitch filter is also included, which is interposed between the output of the Schmitt trigger and the input to the latch. An integrated circuit pin is coupled to both the test mode circuit and to other circuitry on the integrated circuit not forming part of the

L8: Entry 31 of 158 File: USPT Sep 7, 1999

DOCUMENT-IDENTIFIER: US 5950145 A
TITLE: Low voltage test mode operation enable scheme with hardware safeguard

Detailed Description Text (8):
The high voltages on pins WE and A10 are detected by detectors 22, 24, respectively, which may be implemented with known detector circuits. A suitable detector circuit is disclosed in application Ser. No. 08/493,162 filed on Jun. 21, 1995 and entitled INTEGRATED CIRCUIT HAVING HIGH VOLTAGE DETECTION CIRCUIT, the contents of which are hereby fully incorporated into the present application by reference. The outputs of the detectors 22, 24 are used as inputs for OR gates 26, 28, respectively. The outputs of the OR gates 26, 28 are connected to the inputs of an AND gate 30. The output of the AND gate 30 will be high only if the detectors 22, 24 detect high voltages on both the WE and A10 pins. Furthermore, the output of the AND gate 30 is the test mode load enable signal which indicates to the rest of the part that a test mode code may be transferred into the test mode code data latch 42.

Detailed Description Text (15):
FIG. 2 illustrates the detector 22 along with a detector activation logic circuit 52 which may be used in the circuit 20. The detector 22 determines whether a pin has higher voltage than a predetermined voltage, such as 9.0 volts. Since most high voltage detector circuits draw current when enabled, the CE signal is typically used to power up the detectors 22, 24. However, the CE pin toggles to load the test mode codes into the test mode code latch 42 and decoding logic 50. This will result in the output of the detectors 22, 24 switching from HIGH to LOW at the high-going edge of CE, and hence, reset the test mode. To prevent this undesired effect, the detector activation logic 52 is used to ensure that once the output of the detectors 22, 24 are asserted during the test mode, CE is no longer used to power up the detectors 22, 24 and that the test mode is not reset unless WE falls below a predetermined voltage.

CLAIMS:

3. An integrated circuit memory device comprising:

voltage detection circuitry for detecting an externally provided high voltage signal;

a non-volatile latch circuit operable to be programmed to a first state in response to a detected high voltage signal, the non-volatile latch circuit remains in the first state until reset to a second state; and

a test mode circuit for operating the integrated circuit memory device in a high voltage test mode while the detected high voltage signal remains present, and operating the integrated circuit memory device in a low voltage test mode in the absence of the high voltage signal and while the non-volatile latch circuit is in the first state, the low voltage test mode is disabled while the non-volatile latch circuit is in the second state.